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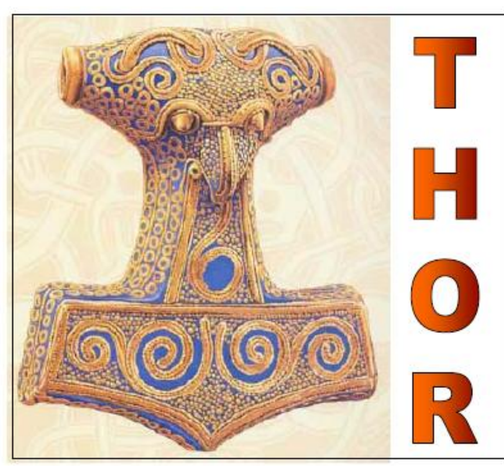

Thermal impact of solder voids in the electronic packaging of power modules

Modelling and simulation of thermal effect on IGBT

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Abstract

In power electronic modules which are used in automotive industry, improving the cooling system is a challenging problem.

In operation mode, the electric current causes an increase of the module's temperature which can have an impact on it's robustness and reliability. The dissipation of heat depends on the quality of the solder joint, which can present some porosity due to the chosen alloy and/or manufacturing process.

In this work, we focus on the impact of solder defects (porosity) on the maximum temperature of the silicon chip. Static thermal analysis was performed using ANSYS code which is based on Finite Element Method (FEM).

Results show an increase of maximum temperature along with the increase of the defect's size (for cylindrical or prismatic void topology). Maximum temperature is controlled by the largest defect in the case of several defects, resulting in localized hot spots.

In order to compare calculations to experimental research, maximum temperature evolution versus porosity is plotted.

Work Package objectives

- Optimize cooling system
- Ultra low dynamical and static losses/Lowest cost
- Highest robustness and reliability
- Minimize external thermal resistances

Keywords

IGBT, simulation, thermal analysis, solder defects, SnPb solder, SAC solder, prismatic and cylindrical defect topology.

Fields of Application

Power Module, Automotive applications

Finite Element Method

Thermal analysis, provided by Mechanical APDL code, was used in order to simulate heat transfer in the component level of the power module.

The heat source is introduced by joule heating, and the cooling system is simulated by convection, with air at the upper -side boundaries and forced liquid flow at the bottom (Table 1).

Figure 1: Simplified structure 3D

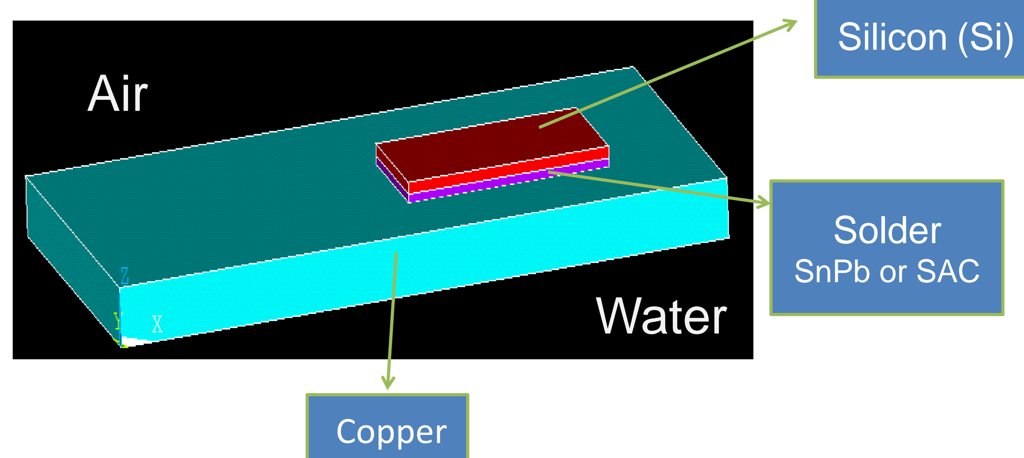


Figure 2: Meshing

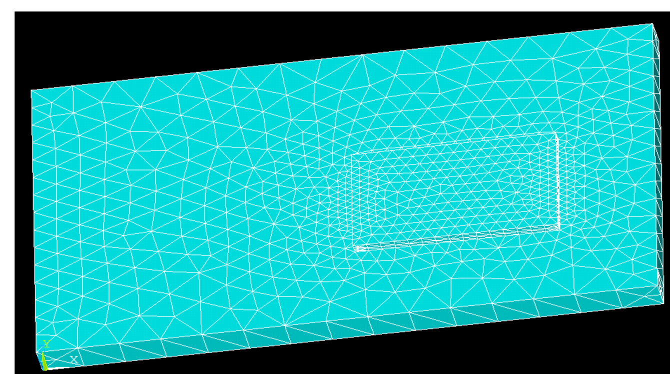


Table 1: Boundary Conditions for convection

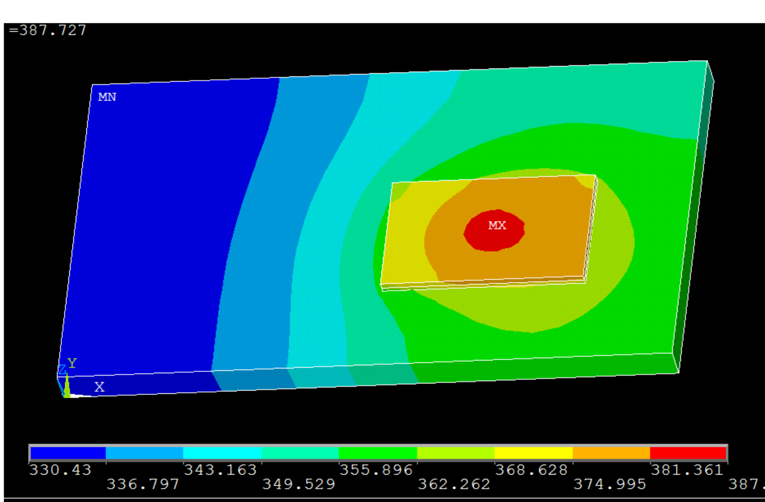
Thermal Boundary Conditions	Heat transfer coefficient W/(m2*K)
Air	5
Forced Water	5000
Reference temperature	293K

Table 2: Electrical Boundary Conditions

Electrical Boundary Conditions	Voltage
Upper boundary of sillicon chip	600 – 1200 V
Bottom boundary of silicon chip	0V

Results of Analysis

Figure 3 : One cylindrical defect - 1200V

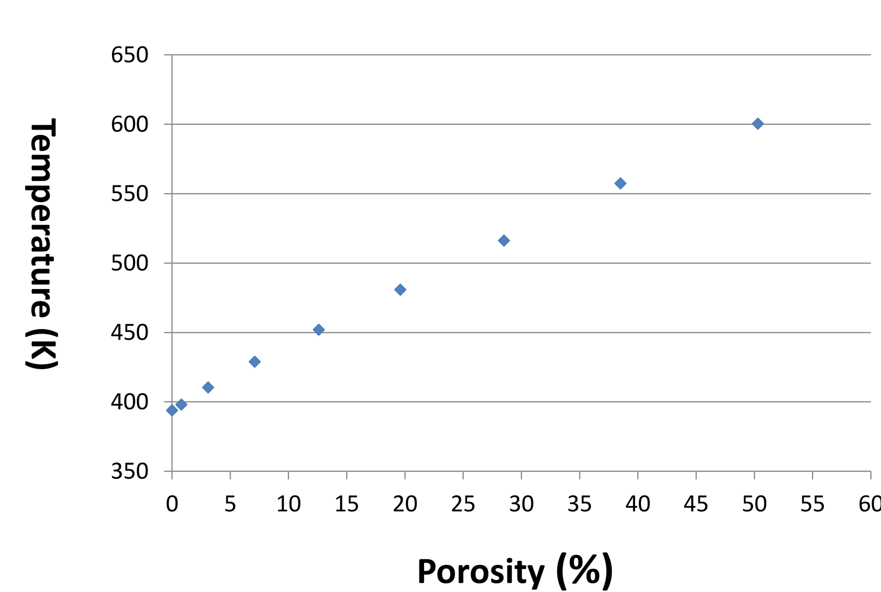


•One defect is centered in the solder joint.

Table 3: Porosity/ MaximumTemperature

Porosity [%]	Maximum Temperature [k]
3.5	387.727
14	405.822
32	433.69

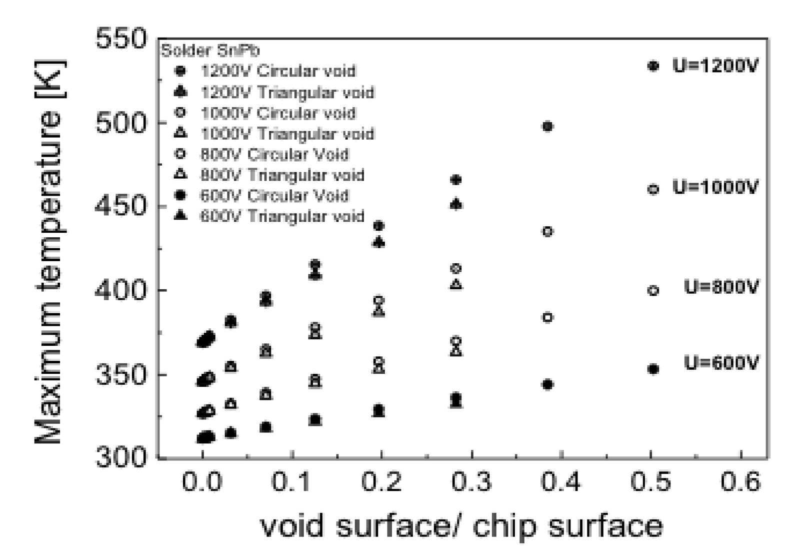
Figure 4 : Tmax [k] versus porosity (%)



•Increasing the porosity of the solder from 0 to 50% leads to a linear increase of the maximum temperature of 200K.

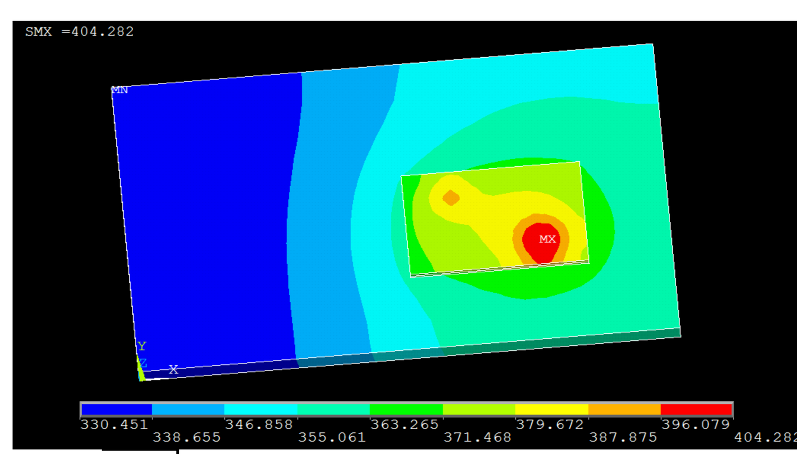
Shape

Figure 5: Maximum Temperature evolution versus void fraction in both cylindrical and prismatic shape



Several defects

Figure 6: 2 cylindrical defects-1200V



Tmax= 404.282 K

Figure 7: Position of defects_porosity

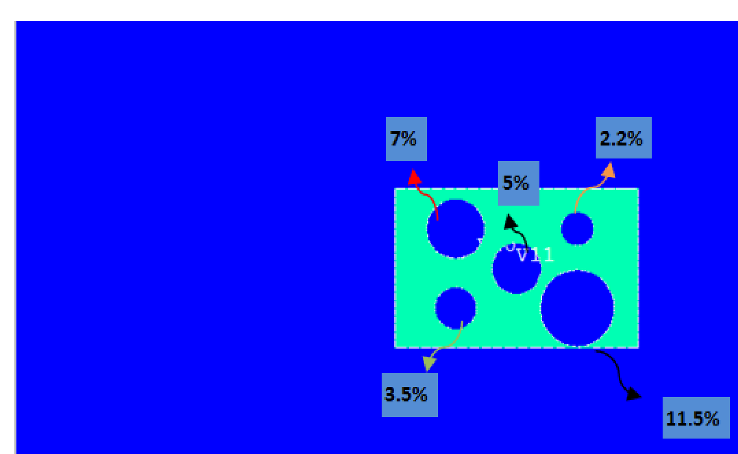
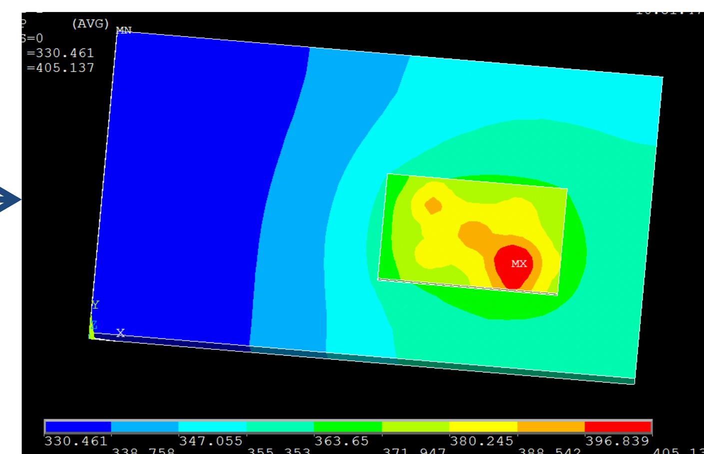


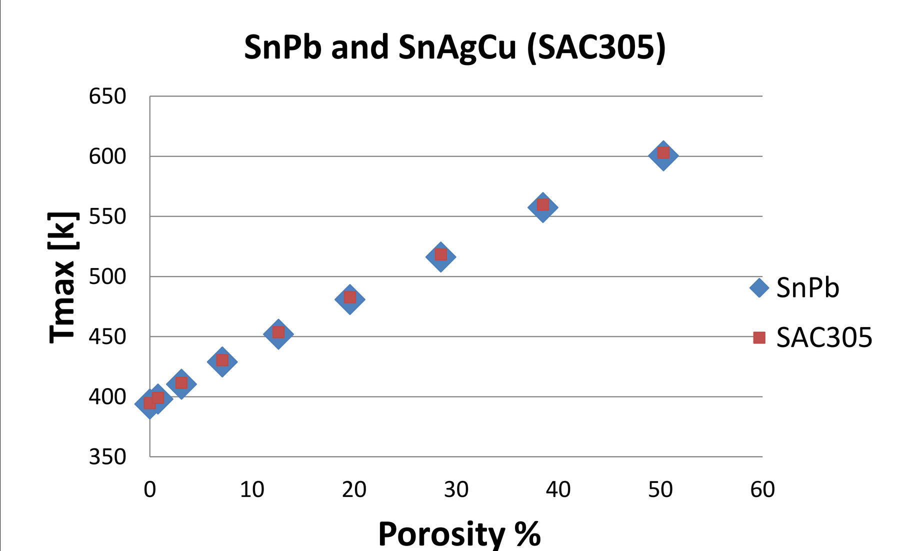
Figure 8: 5 cylindrical defects-1200V



Tmax= 405.137 K

Conclusion : **The maximum temperature is controlled by the largest defect (11.5% porosity).**

Figure 9: **Comparison between solder alloys / one defect case**



Results indicating that there is no significant difference in the maximum temperature between lead alloy (SnPb) and lead-free alloy (SAC).

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